What is claimed is:

1. A multi-layered resist structure comprising:

a lower resist layer formed on a patterning objective layer;

an organic intermediate layer formed on the lower resist layer and made of organic material that contains no Si-O bond; and

an upper resist layer formed on the organic intermediate layer and made of alicyclic resin.

2. A multi-layered resist structure according to claim 1, wherein silicon contained in the organic intermediate layer is bonded only to at least one of hydrogen, carbon, and silicon.

3. A semiconductor device manufacturing method comprising the steps of:

forming a lower resist layer on a patterning objective layer;

forming an organic intermediate layer made of organic material, that contains no Si-O bond in its structure, on the lower resist layer;

forming an upper resist layer made of alicyclic resin on the organic intermediate layer;

forming a pattern by exposing/developing the upper resist layer;

transferring the pattern of the upper resist layer onto the organic intermediate layer by etching the organic intermediate layer while using the upper resist

layer as a mask;

transferring a pattern of the organic intermediate layer onto the lower resist layer by etching the lower resist layer while using the organic intermediate layer as a mask; and

patterning the patterning objective layer by etching the patterning objective layer while using the lower resist layer and the organic intermediate layer as a mask.

4. A semiconductor device manufacturing method according to claim 3, wherein silicon contained in the organic intermediate layer is bonded only to at least one of hydrogen, carbon, and silicon.

5. A semiconductor device manufacturing method according to claim 3, wherein the upper resist layer is exposed by an ArF excimer laser.

6. A semiconductor device manufacturing method according to claim 3, wherein the organic intermediate layer is etched selectively with respect to the lower resist layer.

7. A semiconductor device manufacturing method according to claim 3, wherein the organic intermediate layer is etched simultaneously with etching of the patterning objective layer.

8. A semiconductor device manufacturing method according to claim 3, wherein the upper resist layer is etched and removed simultaneously when the lower resist layer is etched.

9. A semiconductor device manufacturing method according to claim 3, wherein the lower resist layer is formed thicker than a thickness of the patterning objective layer.

10. A semiconductor device manufacturing method according to claim 3, wherein the patterning objective layer is formed of a silicon layer, a silicon substrate, a silicon oxide layer, or a silicon nitride oxide layer.

11. A semiconductor device manufacturing method according to claim 3, wherein the patterning objective layer is a layer on a surface of which an Si-O bond is present, and the lower resist layer is formed of any one of aromatic resin, polyvinylphenol resin, and novolak resin.